# X-Band and Ka-Band Monolithic GaAs PIN Diode Variable Attenuation Limiters

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## ABSTRACT

Monolithic GaAs PIN diode limiter circuits have demonstrated 20 dB of variable attenuation at X- and Ka-bands while maintaining under 1.5:1 input VSWR. Insertion loss is 0.5 dB at 10 GHz and 1.4 dB at 36.5 GHz in the 0-mA bias condition. Passive limiting provides 7 dB of isolation at RF powers up to 1.5 watts (30-percent duty cycle). This paper reports this first use of monolithic GaAs PIN diode circuits in radar receivers.

## INTRODUCTION

FIG. 1 shows the block diagram of a conventional transmit/receiver (T/R) radar module. A variable attenuation limiter between the low-noise amplifier (LNA) and the circulator provides burn-out protection under both transmit and receive conditions. During the transmit mode, the variable attenuation limiter is biased at 15 mA, providing 20 dB of isolation for the LNA. A VSWR of less than 1.5:1 is presented to the circulator, which is required to prevent load pulling of the power amplifier. During the receive mode, the limiter operates at 0-mA bias to achieve minimum insertion loss and provide passive RF limiting protection for the LNA. The process used to fabricate the variable attenuation limiter is compatible with FET circuits, allowing integration of other MMIC components on the same substrate for future single-chip radar front ends. Several of these circuits have been fabricated and RF tested. This paper discusses fabrication, circuit design, and RF performance.

## GaAs PIN DIODE FABRICATION

The surface-oriented diode fabricated on a semi-insulating GaAs substrate allows easy integration into MMICs and is potentially compatible with FET circuits. The semi-insulating substrate serves as the insulating layer (I region) of the PIN diode.

The fabrication process for the PIN diode, as outlined in Fig. 2, begins with deposition and patterning of silicon nitride ($Si_3N_4$) on the undoped substrate [Fig. 2(A)]. This pattern defines both the $p^+$ and $n^+$ regions of the PIN diode, which results in self-alignment of the $p^+$ and $n^+$ regions for excellent control of the width of the I region. A trench is etched in the GaAs to a depth of 1 $\mu$m [Fig. 2(B)]. The trench allows the

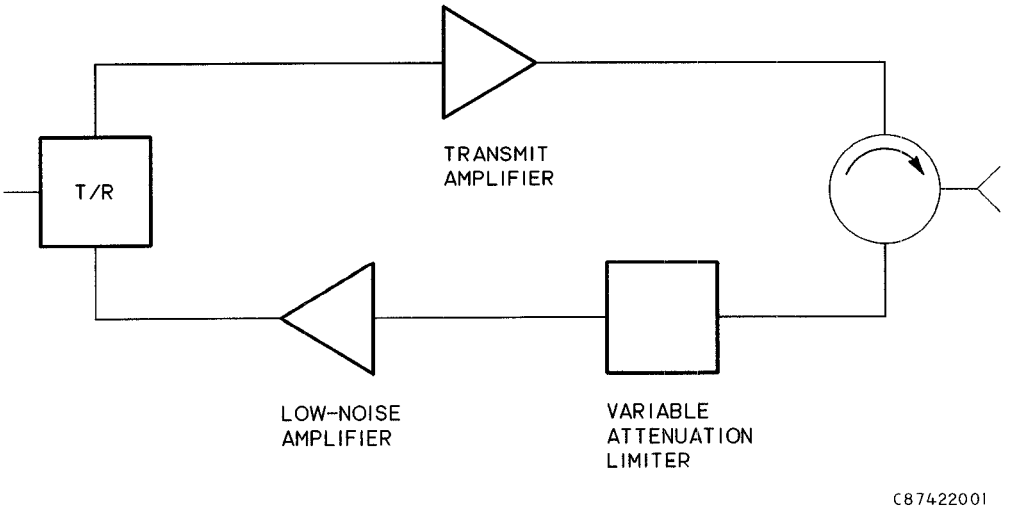


**Fig. 1. Simplified radar module block diagram**



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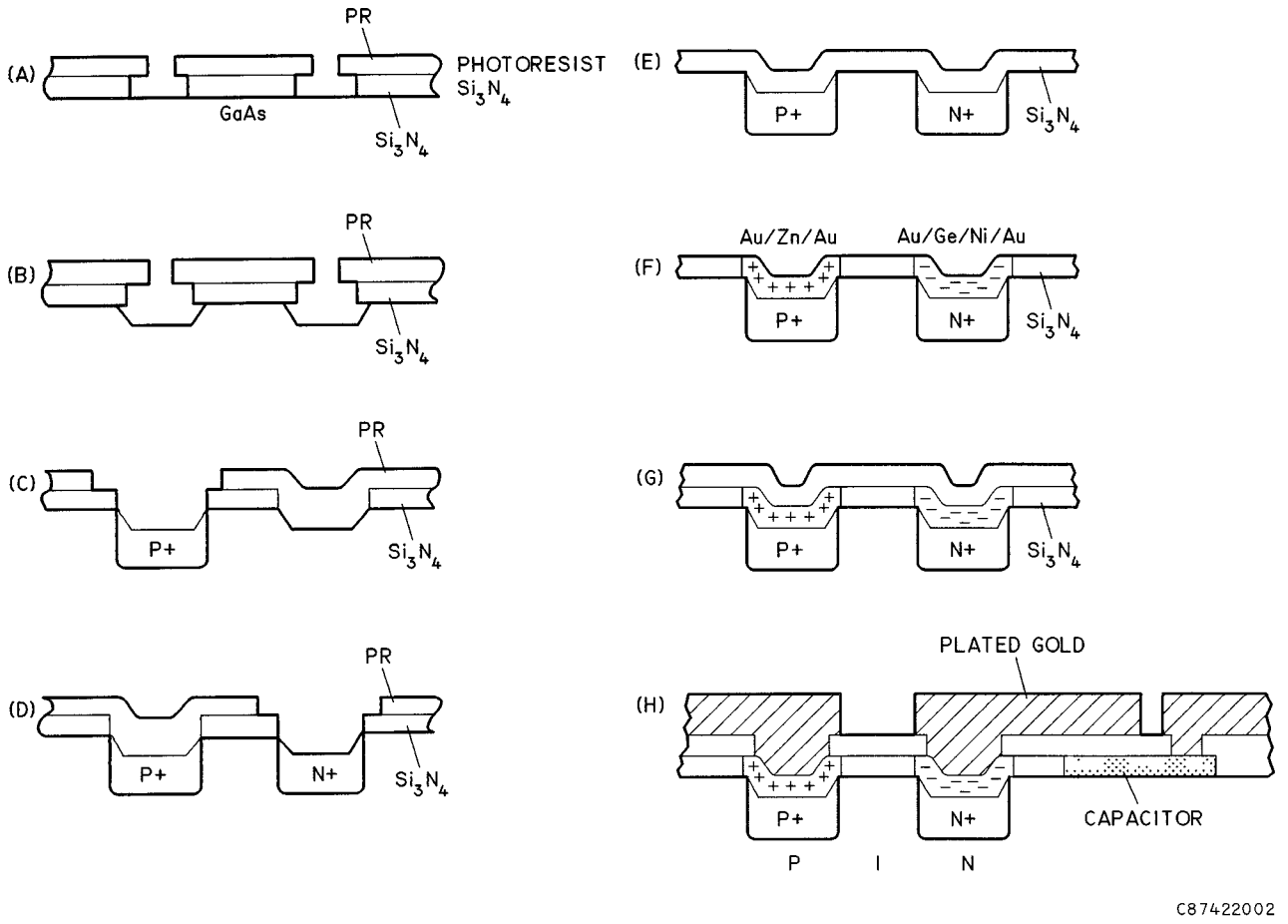


**Fig. 2. GaAs monolithic pin diode fabrication steps**

sidewalls of the $p^+$ and $n^+$ regions to have larger areas, resulting in higher carrier injection. This reduces the series resistance by a factor of 3. The resist is removed and another resist layer is applied and patterned [Fig. 2(C)].

This second resist acts as a mask for the Be implant in the $n^+$ region. The nitride serves as the implant mask of the Be into the $p^+$ region. The self-alignment of the implant to the trench ensures good control of the PIN diode spacing. The resist is removed and the previous step is repeated for the Si implant [Fig. 2(D)]. The Si implant is the same as for a low-noise FET, implying future integration of low-noise FETs on the same circuit. After both implants are completed, the resist and nitride are removed. The slice is annealed using an undoped cover slice in a proximity anneal for 15 minutes at 850°C. After anneal, the GaAs slice is covered with 3,000 Å of $Si_3N_4$. The contact metals for the $p^+$ are 3,000 Å of Au/Zn/Au and for the $n^+$ are 3,000 Å of AuGe/Ni/Au. After the contact metals are alloyed, Ti/Pt/Au is patterned and lifted off. The Ti/Pt/Au serves as capacitor bottom plate and first level metal [Fig. 2(E)]. After the metals have been patterned, 2,000 Å of $Si_3N_4$ are deposited. This nitride serves as the dielectric for capacitors and circuit crossovers [Fig. 2(G)]. The last step is the deposition of the top metal layer to form interconnects and transmission lines [Fig. 2(H)].

## RF Design

Fig. 3 shows the circuit schematic of the variable attenuation limiter. Low insertion loss is obtained in the 0-mA bias condition by resonating the off-capacitance of the shunt PIN/NIP combination with a high-impedance transmission line. Variable attenuation levels are achieved through biasing of the load PIN diodes and the shunt PIN diode. The diode impedance is current-dependent and results in a continuously variable attenuation. The diodes are scaled to provide input VSWR less than 1.5:1.

## RF Performance

Fig. 4 is a photograph of the X-band variable attenuation limiter circuit. RF performance versus bias current is shown in

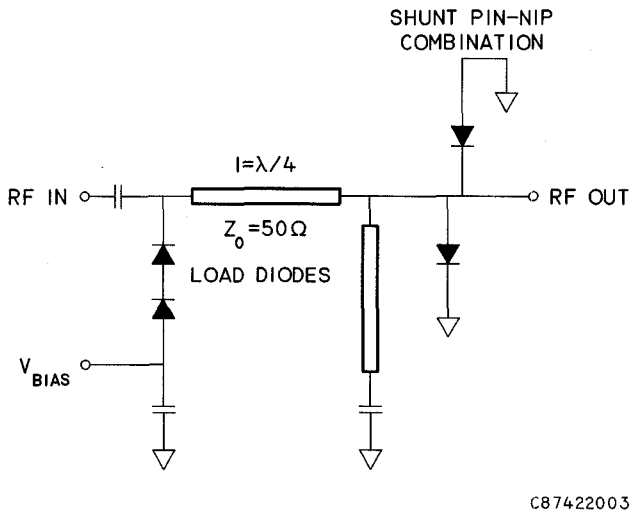


**Fig. 3. Monolithic pin diode variable attenuation limiter schematic**

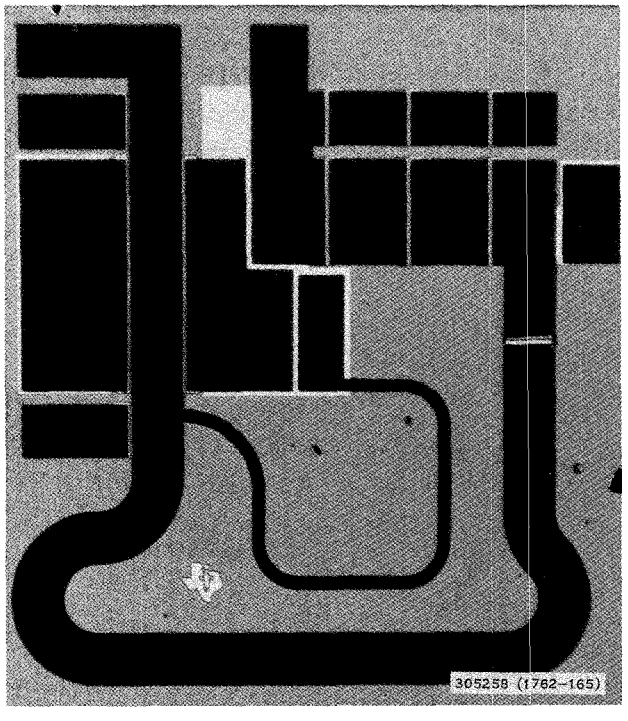


**Fig. 4. X-band variable attenuation limiter**

Table I. Insertion loss and maximum input VSWR are recorded for a 7.2- to 10.2-GHz band. From 9.2 to 10.2 GHz, 0-mA bias insertion loss is under 0.5 dB, and 20 dB of variable attenuation is achievable with less than 1.5:1 input VSWR.

TABLE I. VARIABLE ATTENUATION LIMITER RF PERFORMANCE (7.2 TO 10.2 GHz)

| Bias (mA) | Insertion Loss (dB) | Input VSWR |
|---|---|---|
| 0 | 0.49 ±0.11 | 1.43 |
| 5 | 10.04 ±0.31 | 1.36 |
| 10 | 15.29 ±0.36 | 1.46 |
| 15 | 19.36 ±0.40 | 1.73 |

Fig. 5 is a photograph of the Ka-band variable attenuation limiter circuit, Fig. 6 shows 0-mA bias insertion loss and return loss, and Fig. 7 shows RF performance at 20-mA bias current. At 36.5 GHz, 0-mA bias insertion loss is 1.4 dB, and over 20 dB of variable attenuation is achievable.

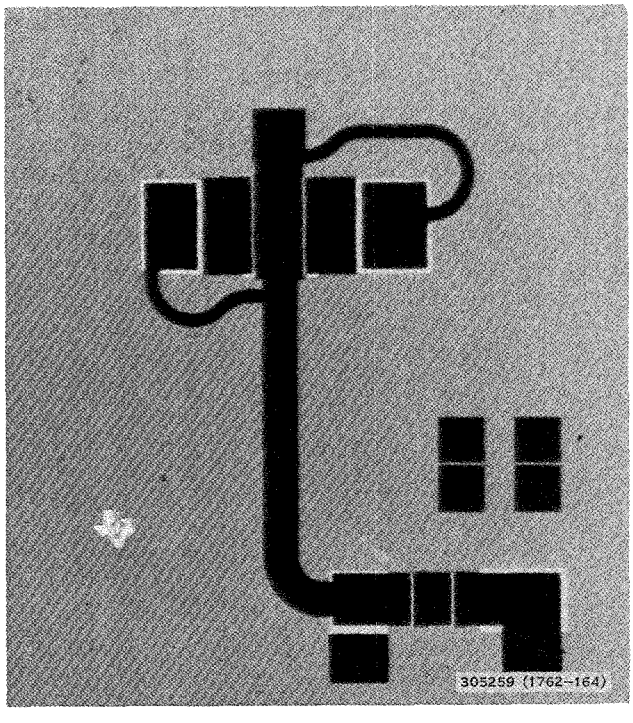


**Fig. 5. Ka-band variable attenuation limiter**

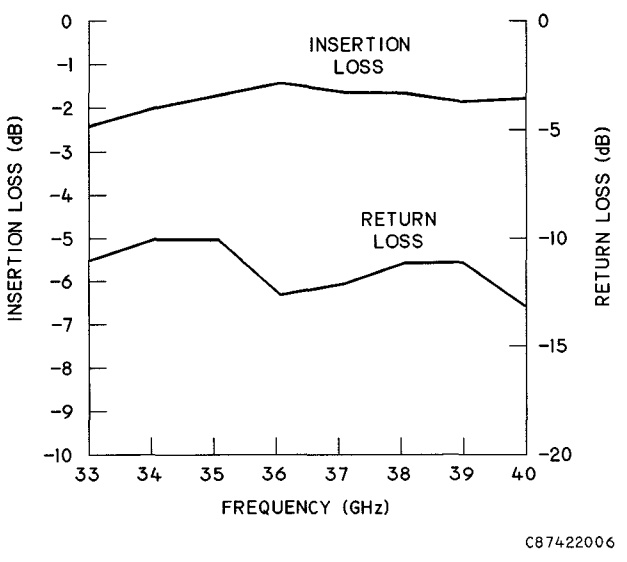


**Fig. 6. Ka-band variable attenuation limiter 0-bias performance**

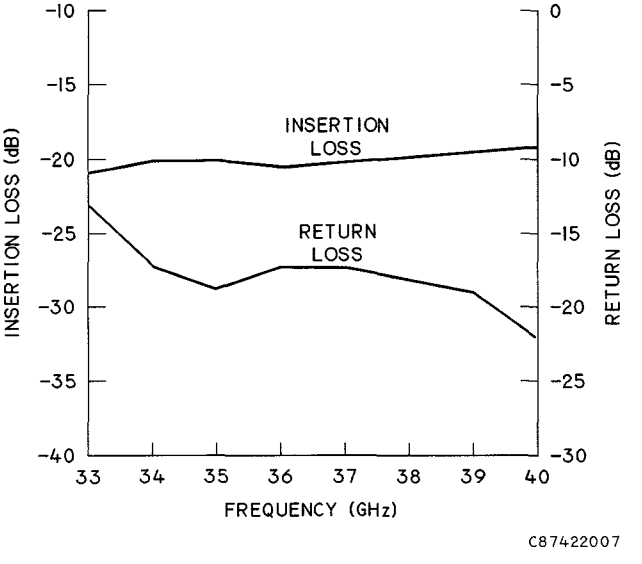


**Fig. 7. Ka-band variable attenuation limiter 20-mA performance**

## CONCLUSIONS

Monolithic GaAs PIN diode technology is capable of performing multifunction circuit roles in radar receivers with state-of-the-art performance as demonstrated by X-band and Ka-band variable attenuation limiters. This technology is compatible with FETs for future higher level integration of circuit complexity.

## ACKNOWLEDGMENTS

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